REMARKS

Applicants respectfully traverse and request reconsideration. In conjunction with this preliminary amendment, Applicants submit a Request for Continued Examination (RCE).

Claims 1–10, 12–19 and 21–22 are rejected under 35 U.S.C. § 103(a) based on U.S. Patent Number 6,446,193 (Alidina), in view of Gregory T. Byrd, "Multithreaded Processor Architectures," IEEE SPECTRUM August 1995 (Byrd).

In the response to the final Office Action, the Applicants asserted confusion because of contradictory statements made in the Office Action. According to the Advisory Action, the Office Action incorrectly asserted that Alidina teaches the preamble of claim 1 and "an accumulation circuit that supports a plurality of threads." According to the Advisory Action, the assertion that Alidina teaches the claimed plurality of threads is a typographical error. However, the Advisory Action failed to address the Applicant's arguments regarding the lack of a *prima facie* case of obviousness. The Office Action continues to acknowledge that Alidina neither teaches (1) multi-threading (2) nor has registers and (3) operands that correspond to each individual thread. (Office Action, page 3, ref. #5; page 4, ref. #6; page 8, ref. #16; page 10, ref. #20; page 12, ref. #23; page 15, ref. #28.) Since the office action acknowledges that Alidina fails to teach multi-threading and having registers and operands which correspond to each individual thread, the office action acknowledges that Alidina fails to teach, among other things, the following italicized portions of claim 1:

> 1. A *multi-thread* accumulation circuit that supports a plurality of threads, comprising:
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> a first operation unit operably coupled to receive a first operand and a second operand corresponding to an operation code issued *by a selected thread of the plurality of threads*, wherein the operation unit combines the first and second operands to produce a first operation result *corresponding to the selected thread*;
>
> a plurality of accumulation registers operably coupled to the first operation unit, *wherein each accumulation register of the plurality of accumulation registers corresponds to one of the plurality of threads, wherein a selected accumulation register that corresponds to the selected thread stores the first operation result corresponding to the selected thread*; and

a selection block operably coupled to the plurality of accumulation registers and the first operation unit, wherein the selection block selects the second operand provided to the first operation unit from a set of potential operands, *wherein the set of potential operands includes contents of each accumulation register of the plurality of accumulation registers.*

Alidina, throughout the specification, repeatedly describes performing concurrent operations on a parallel processing system rather than multi-threaded operations. (Alidina, Col. 1, lines 13–14, lines 60–63; Col. 2, lines 41–42; Col. 3, lines 39–43; Col. 4, lines 22–24.) For example, Alidina describes performing concurrent operations on a parallel processing system in a single processor cycle instead of two cycles. (Alidina, Col. 2, lines 54–56; Col. 3, lines 10–11, lines 25–27; Col. 6, line 44.) Alidina also explicitly seeks to achieve the performance of one scale and load/store operation every cycle. (Alidina Col. 6 lines 14-18.) Further, Alidina specifically teaches a parallel processing system using two multiply-accumulate (MAC) processors which concurrently multiply two values, then add the resulting value to another and accumulate the result. (Alidina, Col. 1, lines 49–54, Col. 1, lines 61–63.) Alidina explicitly teaches that the parallel processing system advantageously reduces the number of instruction cycles and enhances the MIPs (millions of instructions per second) number by freeing up valuable instruction time for other operations. (Col. 3, lines 49–52.). (Emphasis added). Since multi-threading relates to processing serially, rather than in parallel, multi-threading does not reduce the number of instructions to enhance total MIPs. As a result, Alidina teaches away from multi-threading. Further, since Alidina teaches concurrent processing in order to reduce the number of instruction cycles, Alidina explicitly teaches away from multi-threading since multi-threading would require processing instructions one at a time rather than concurrently.

Byrd as cited, is directed to "multi-threaded processor architectures," namely "independent streams of instructions, interwoven on a *single processor*, to fill its otherwise idle cycles and so boost its performance." (Byrd, page 38, title and side bar, lines 9–10. (emphasis added). Therefore, Byrd as cited, teaches multi-threading by interweaving processes on a single processor. For example, as shown on page 39 (lower left corner) Byrd explicitly teaches a time-line chart for processing one thread at a time on a single processor rather than in parallel.

The combination of Alidina and Byrd is not proper because such an attempt to combine these references would teach the contradictory requirements of modifying parallel processors

coupled to a single optimized register set for performing concurrent plural operations, into a single processor for processing one thread at a time and adding a plurality of registers corresponding to each thread. Therefore, modifying Alidina with the teachings of Byrd as suggested in the Office Action would destroy at least the three main principles of Alidina, namely, (1) where Alidina teaches the execution of concurrent operations to enhance MIP performance and achieve one scale and load/store every cycle, Byrd as cited on page 38 instead teaches interleaved processing one thread at a time, resulting in multiple cycles to achieve a scale and load/store rather than one cycle, (2) where Alidina teaches two processors for concurrent processing, Byrd as cited instead teaches a single processor for processing instructions one at a time, and (3) where Alidina teaches processing on a single register for efficient processing thus maximizing MIPs (Col. 2, lines 20-23 and 65), Byrd instead teaches multiple sets of general purpose registers. As a result, Byrd fails to compensate for Alidina's shortcomings. Despite explicit teachings to the contrary, the Office Action argues that one would be motivated to change the fundamental principles of Alidina, which relate to concurrent (parallel) execution of operations on a dual processor using a single register, with Byrd's teaching of interleaved processing on a single processor using multiple registers.[1] Despite the explicit teachings of Byrd and Alidina, the Office Action inexplicably and without support continues to maintain that one would be motivated to modify each of the fundamental attributes of Alidina with fundamentally opposite attributes of Byrd as described above. Further, if Alidina were modified by Byrd as suggested in the office action, such a modification would destroy the resulting performance advantage of one scale and load/store every cycle specifically sought by Alidina because multi-threading would result in a scale and load/store occurring in more than one clock cycle.[2] (Alidina Col. 6 lines 14-18.) Therefore, the combination of Alidina and Byrd do not function in the same way to obtain the same result as the claimed invention. For at least these reasons, the Office Action fails to show sufficient motivation to combine the references and, therefore, the Office Action fails to establish a *prima facie* case of obviousness.

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[1] If the proposed modification or combination of the prior art would change the principle of operation of the prior art invention being modified, then the teachings of the references are not sufficient to render the claims *prima facie* obvious. *In re Ratti*, 270 F.2d 810, 123 U.S.P.Q. 349 (CCPA 1959). See M.P.E.P. 2143.01.

[2] If the proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification. *In re Gordon*, 733 F.2d 200, 221 USPQ 1125 (Fed. Cir. 1984), MPEP 2143.02.

In contrast, claim 1 recites, among other things, "a first operation unit operably coupled to receive a first operand and a second operand corresponding to an operation code issued by a selected thread of the plurality of threads, wherein the operation unit combines the first and second operands to produce a first operation result corresponding to the selected thread." Applicants note that the office action fails to show or cite to where either Alidina or Byrd teach, among other things, "a first operation unit operably coupled to receive a first operand and a second operand corresponding to an operation code issued *by a selected thread of the plurality of threads*, a selected thread", and "wherein the operation unit combines the first and second operands to produce a first operation result corresponding to the selected thread." Instead, the office action merely cites to four pages of Byrd without particularly pointing to or citing to Byrd and therefore fails to explain with specificity how each claim is rejected. M.P.E.P. 706, C.F.R. § 1.104(c)(2). A corresponding showing is requested.

Further, claims 1, 12 and 17 recite, among other things: a plurality of accumulation registers operably coupled to the first operation unit, wherein each accumulation register of the plurality of accumulation registers correspond to one of the plurality of threads, wherein a selected accumulation register that corresponds to the selected thread stores the first operation result corresponding to the selected thread. The office action also does not even show or cite where the combination of Alidina and Byrd teaches, among other things, "wherein each accumulation register of the plurality of accumulation registers corresponds to one of the plurality of threads" and "wherein a selected accumulation register that corresponds to the selected thread stores the first operation result corresponding to the selected thread." Instead, the office action merely cites to four pages of Byrd and as a result fails to explain with specificity how each claim is rejected. M.P.E.P. 706, C.F.R. § 1.104(c)(2). Therefore, the Office Action fails to establish a *prima facie* case of obviousness because the Office Action fails to show how each and every element in the claims is taught by the references. If the Office Action maintains the rejection, a corresponding showing of where Alidina and Byrd teaches each element as arranged in the claims is requested. Reconsideration and withdrawal of the rejection with respect to claims 1, 2 and 17 is respectfully requested.

According to the Office Action on page 20, paragraph number 40, "Alidina was used to show the components of a typical digital signal processor." However, as stated above, Alidina instead teaches a dual processor performing parallel operations in a single cycle rather than a

multi-thread accumulation circuit.[3] As a result, the Office Action appears to have misinterpreted Alidina since the Office Action characterizes Alidina merely as a typical digital signal processor where Alidina actually teaches a specific dual processor architecture for performing parallel operations in a single cycle. Therefore, Alidina teaches away from multi-threading.

According to the response to arguments in the Office Action on page 18, Byrd was combined with Alidina to teach multiple threads, saving data and information, like the accumulation register of a thread. However, as described above and as described previously in the response to the prior Office Action, Alidina explicitly teaches a dual processor performing parallel operations in a single cycle rather than multi-threading, and therefore teaches away from the claims and Byrd. (Alidina, Col. 2, lines 60–65.) Further, as shown in Fig. 3, Alidina explicitly teaches a single set of accumulation registers for MAC operations rather than at the claimed plurality of accumulation registers, wherein each accumulation register corresponds to one of a plurality of threads. Alidina similarly explicitly avoids the use of additional accumulators because, where the number of accumulators becomes large, processing efficiency decreases and further decreases MIPs. (Alidina, Col. 2, lines 20–23.) For at least the reasons above, one would not be motivated to modify the parallel processor architecture of Alidina for performing concurrent operations since multi-threading would greatly increase processing complexity and destroy the performance gains sought in a parallel processor environment. Modifying the dual processor computer system of Alidina with the single processor system of Byrd to perform threaded-type operations would destroy the performance advantages explicitly sought to be achieved in Alidina.

According to the response to the arguments section on page 19, paragraph 38, the Office Action argues that if the prior art structure is capable of performing the intended use of multi-threading, then it meets the claim. However, for at least the reasons provided above, since Alidina is explicitly directed to a parallel processor architecture for performing parallel operations in a single instruction, Alidina does not appear to be intended for multi-threading instructions on a plurality of accumulation registers. Therefore, modifying Alidina as suggested would destroy Aladina's principle of operation and as a result, Alidina teaches away from threading and further, Alidina teaches away from modification by Byrd. Since insufficient

[3] A prior art reference must be considered in its entirety, i.e. as a whole including portions that would lead away from the claimed invention. (*W.L. Gore & Associates, Inc. v. Garlock, Inc.*, 721 F.2d 1540, 220 USPQ 303 (Fed.

motivation exists to modify Alidina with Byrd as suggested in the Office Action, the Office Action fails to establish a *prima facie* case of obviousness. Applicants respectfully request reconsideration and withdrawal of the present rejection.

Claims 11 and 20 are rejected under 35 U.S.C. §103(a) based on Alidina in view of Byrd and further in view of United States Patent No. 5,673,377 ("Berkaloff"). The office action acknowledges that Alidina does not explicitly teach "wherein the first register section accumulates diffuse color information corresponding to graphics primitives, and wherein the second register section accumulates specular color information corresponding to the graphics primitives." Further, Applicants repeat the above remarks, especially those that teach that the references, even if combined, fail to teach, among other things, multi-threading and further teach away from multithreaded systems. Nevertheless, the office action asserts that Alidina teaches DSP processors that are optimal for certain graphical and audio operations. (Office Action, page 17, ¶33.) However, Alidina instead appears to be directed towards the analysis of analog sound signals (col. 1, lines 16–18) and speech coding. (Alidina, col. 4, lines 57–69.) In direct contradiction to the assertion in the office action, Alidina appears to be silent with respect to graphical operations. Further, the assertion in the office action that it would have been obvious to one of ordinary skill in the art to incorporate the color information of Berkaloff, because it is needed in the calculations to create effective images, is circular, and therefore fails to provide sufficient motivation for one skilled in the art to modify the teachings of Alidina for Byrd. Since the office action fails to show how each and every element of the claims is taught by the combination of the references and also since insufficient motivation exists to modify Alidina and Byrd with the teachings of Berkaloff, as suggested in the office action, the office action fails to establish a *prima facie* case of obviousness. Applicants respectfully request reconsideration and withdrawal of the present rejection.

Dependent Claims 2–11, 13–16, 18–20 and 22

Applicants submit that the dependent claims are allowable in light of the presence of novel and non-obvious elements contained in these claims that are not otherwise present in independent claims 1, 12, 17 and 21. Therefore, these claims are allowable for at least the reasons the independent claims and any intermediate claims are allowable.

Cir. 1983), cert. denied, 469 U.S. 851 (1984) MPEP 2141.02.)

Support for new claims 23 and 24 may be found in original claims 12 and 16. New claims 23 and 24 are allowable for at least the reasons the independent claims and any intermediate claims are allowable.

CONCLUSION

Applicants respectfully submit that the claims are in condition for allowance and respectfully request that a timely notice of allowance be issued in this case. The Examiner is invited to contact the below-listed attorney if the Examiner believes that a telephone conference will advance the prosecution of this Application.

Respectfully submitted,

By _____
Themi Anagnos
Reg. No. 47,388

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Vedder, Price, Kaufman & Kammholz, P.C.
222 North LaSalle Street
Chicago, Illinois 60601
PHONE: (312) 609-7970
FAX: (312) 609-5005

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